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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,250	08/02/2001	James J. O' Brien	2000.034/1109.008	8709

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	7

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/921,250	Applicant(s) O' BRIEN, JAMES J.	
	Examiner Nadeem Iqbal	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-34* is/are allowed.

6)☐ Claim(s) *1-5,7,8,10-31* is/are rejected.

7)☐ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7, 8, 10-12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya, (U.S. Patent number 6381717), in view of Brannick et al., (U.S. Patent number 6289300).

3. As per claim 1, Bhattacharya teaches (col. 2, lines 12-14) a test access port controller and a programmable switch control testing of the electronic circuits. The programmable switch is controlled to selectively connect the first the first test access port to the embedded core circuits. He thus teaches limitations pertain to a method of emulating individual devices, obtaining topology of the chain, selecting one device within the chain, placing at least one other device into bypass mode. He does not explicitly discloses sending emulation instructions to the chain, wherein the emulation instructions bypass the at least one other device and are executed by the one device. Brannick et al., teaches (col. 38-40) an emulation system for use with an integrated circuit. He also teaches a serial data link that utilizes a pin that may be used as a communication link between emulation system and an external development system. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Bhattacharya's access port controller to include the emulation system of Brannick to send

emulation instructions to the chain of circuits of Bhattacharya. This is because Bhattacharya already teaches a test access port controller and a programmable switch control testing of the electronic circuits and the inclusion of Brannick emulation system clearly would enable emulation instructions to be sent to the chain of circuits for emulating circuits of Bhattacharya, thus providing motivation for the stated inclusion.

4. As per claim 2, Bhattacharya teaches (col. 2, lines 6-8) testing technique for electronic circuits that includes test access port and compliant with the IEEE standard 1149.1, therefore would include JTAG devices and a boundary scan chain.

5. As per claim 3, Bhattacharya teaches a programmable switch is controlled to selectively connect the first the first test access port to the embedded core circuits and with combination with Brannick emulation system as stated per claim 1 above would provide the selecting and placing effected by the emulator.

6. As per claim 4, Brannick teaches a communication link between emulation system and an external development system, therefore would send the selection instructions to the scan chain.

7. As per claim 5, Brannick teaches (col. 3, lines 3-5) that the data processor executes emulation instructions using reserved emulation registers, therefore would include register to receive the selection instruction.

Allowable Subject Matter

8. Claims 32-34 are allowed.

9. Claims 6 & 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. As per claim 7, Bhattacharya teaches a programmable switch is controlled to selectively connect the first test access port to the embedded core circuits and with combination with Brannick emulation system as stated per claim 1 above would provide the selecting and placing effected by the emulator.

11. As per claim 8, Brannick teaches (col. 3, lines 3-5) that the data processor executes emulation instructions using reserved emulation registers, therefore would include register to receive the bypass instruction.

12. As per claims 10-12, As stated per claim 1 above Bhattacharya already teaches a test access port controller and a programmable switch control testing of the electronic circuits and the inclusion of Brannick emulation system clearly would enable emulation instructions to be sent to the chain of circuits.

13. Claims 13-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhattacharya, (U.S. Patent number 6381717), in view of Brannick et al., (U.S. Patent number 6289300) as applied to claims 1-5, 7, 8, 10-12 above, and further in view of Ryan et al., (U.S. Patent number 6389565).

14. As per claims 13 & 16, Bhattacharya does not explicitly disclose automatically determining the topology of the scan chain. Ryan teaches (col. 3, lines 5-7) a user interface that allows a user to view boundary scan test data generated by a boundary scan testing device in a format well-suited for debugging. The formatting and data generation of Ryan would require determining automatically the topology of the scan chain. A person of ordinary skill in the art would have been motivated to include Ryan's invention into Bhattacharya since both inventions

are in the same environment of boundary scan and the stated inclusion provides a desirable advantage of displaying boundary scan test data.

15. As per claims 14 & 15, Brannick teaches (col. 3, lines 3-5) that the data processor executes emulation instructions using reserved emulation registers, therefore would include register bits in each of the devices.

16. As per claim 17, Brannick teaches an emulator debugger that performs debugging functions; therefore the combination with Bhattacharya would provide a debugger.

17. As per claims 18 & 19, Ryan teaches (col. 3, lines 5-7) a user interface that allows a user to view boundary scan test data generated by a boundary scan testing device.

18. As per claims 20 & 21, Ryan teaches (col. 3, lines 11-14) that the user views the frame cell number in the boundary scan chain, the device name, the pin of the device associated with the cell, the node associated with the pin.

19. As per claim 22, Brannick teaches an emulator debugger, that performs debugging functions, therefore the combination with Bhattacharya would provides coupling an emulator to the chain.

20. As per claims 23 & 24, Ryan teaches (col. 3, lines 5-7) a user interface that allows a user to view boundary scan test data generated by a boundary scan testing device in a format well-suited for debugging. He also teaches (col. 3, lines 11-14) that the user views the frame cell number in the boundary scan chain, the device name, the pin of the device associated with the cell, the node associated with the pin. He thus teaches limitations in this claim.

21. As per claims 25 & 26, Ryan also teaches (col. 3, lines 11-14) that the user views the frame cell number in the boundary scan chain, the device name, the pin of the device associated with the cell, the node associated with the pin. He thus teaches limitations in these claims.

22. As per claims 27 & 28, Ryan teaches (col. 3, lines 5-7) a user interface that allows a user to view boundary scan test data generated by a boundary scan testing device. Ryan also teaches (col. 3, lines 11-14) that the user views the frame cell number in the boundary scan chain, the device name, the pin of the device associated with the cell, the node associated with the pin. He thus teaches limitations in these claims.

23. As per claims 29-31, Bhattacharya substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 2, lines 12-14) a test access port controller and a programmable switch control testing of the electronic circuits. The programmable switch is controlled to selectively connect the first the first test access port to the embedded core circuits. He thus teaches limitations pertain to a method of emulating individual devices, obtaining topology of the chain, selecting one device within the chain, placing at least one other device into bypass mode. He does not explicitly discloses sending emulation instructions to the chain, wherein the emulation instructions bypass the at least one other device and are executed by the one device. Brannick et al., teaches (col. 38-40) an emulation system for use with an integrated circuit. He also teaches a serial data link that utilizes a pin that may be used as a communication link between emulation system and an external development system. It would have been obvious to a person of ordinary skill in the art to modify Bhattacharya's access port controller to include the emulation system of Brannick to send emulation instructions to the chain of circuits of Bhattacharya. This is because Bhattacharya already teaches a test access port

controller and a programmable switch control testing of the electronic circuits and the inclusion of Brannick emulation system clearly would enable emulation instructions to be sent to the chain of circuits for emulating circuits of Bhattacharya, thus providing motivation for the stated inclusion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI